UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/584,604	05/31/2000	Scott A. Rosenberg	INTL-0364-US (P8583)	2847

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DATE MAILED: 11/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,9-11,13-17 and 19-25* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9-11,13-17 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☒ Interview Summary (PTO-413) Paper No(s). *10* .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

Response to Arguments

Applicant's arguments filed on August 18, 2003 in response to the office action mailed on

July 2, 2003, have been fully considered but they are not persuasive.

Applicant fails to response completely to the office action, on page 2-4.

Overlooked questions from the office action mailed on July 2, 2003 are as following:

1.   In regard to phrase "one-way re-mapping", on page 2.

   a.   Applicant fails to describe or illustrate how does the phrase "one-way re-

mapping" function?

2.   In regard to terms "first, second and a virtual memory", on page 2.

   b.   Applicant does not specify the significant (shown with underline) of the

transformation of pixel data from <u>a first to a second memory location in a virtual memory</u>

<u>space</u>?

   c.   Applicant does not explicitly specifying the advantages of claiming first and

second memory locations, because the amount of addressable location can be divided into

first, second and etc. locations in memory?

   d.   The applicant does not explicitly specifying how the data is transferred?

3.   In regard to "passive engine", on page 3.

   e.   Applicant does not disclose, how does the "passive engine" operate?

   f.   Why applicant does not show "passive engine" in the specification?

   g.   Does the "passive engine" affect the performance of memory location?

4.   In regard to terms "writing/performing/generating/transferring commands", on page 4.

   h.   Applicant does not claim how the data is obtained?

    i.   Where does the specification show the method of write/perform/generate and

transfer command?

Response to remarks on page 2:

➢ Applicant on page 2, argues that the reference Patrick fails to teach use of a one-way re-

mapping to write the transformed pixel data from the first virtual to the second virtual

memory location. Examiner's reply: Applicant fails to provide explanations for the

phrase "one-way re-mapping", in order the Examiner provides any interpretation!

➢ Applicant on page 2, lines 16-21, argues that Patrick fails to map of the transfer functions

including the first pixel transformation at the first virtual memory location in the virtual

memory space. Examiner's reply: Knowing that the Virtual memory is extension of the

computer's internal memory, it considers locally or remotely. Examiner's interpretation

from given information in the specification and from the claim: Applicant claims the

image data are stored in the memory. Applicant fails to specify explicitly the significant

of mapping of the transfer functions.

➢ Applicant on page 2, lines 22-25, argues the Patrick and Margulis fail to provide mapping

of the transfer function onto a virtual memory space in parallel instead of serially. And

Applicant refers Examiner to see col. 5, lines 33-35 and col. 6, lines 29-30 of Patrick.

Examiner's reply: Patrick in col. 5, lines 33-35 discloses the rate of transfer is increased

by transferring the data block in groups of multiple bytes, where possible, such as in 2- or

4-byte groups. And also Patrick in col. 6, lines 29-30 discloses each byte in data block

must be fetched (i.e., read) from a source address and written to a destination address.

Patrick on col. 13, lines 45-51, discloses that the preferred embodiment the raster routine

applies the ROP to 4 bytes (or entire 32-bit registers), rather than to 1 byte as in previous versions. This implementation is 4 times faster because all 4 bytes are done in parallel, or in the same amount of time it previously took to work perform the raster operation on 1 byte.

➢ Applicant on page 3, lines 8-15, argues that Margulis merely teaches use of a mapping policy for locating one or more row buffers corresponding to the memory locations. Examiner's reply: Margulis in paragraph 0060 discloses that an implementation detail for the allocation of row buffers corresponding to the memory locations is the tradeoff between performance and simplicity of implementation. In the simplest case, a row buffer is "direct mapped" to a fixed number of potential memory array rows. In the most flexible and most complex case, any row buffer corresponds to any IDRAM row and is said to be "fully associative." Intermediate complexity of design of a "set associative" mapping is possible where more than one row buffer corresponds to each fixed set of IDRAM rows. And also Margulis in paragraph 0075 discloses that in the case where multiple GDPs are rendering data, the rendered data is not always in a regular structure representing a frame buffer. The Display Processor Subsystem (DPS) can be provided with the mapping information and reconstruct the display information from the various stored rendering information. The DPS reconstructs the image scan line-by-scan line so that the data can be sent out and displayed properly. The DPS also performs operations such as scaling and filtering that are better suited to being performed in this back end path than by the GDPs.

Applicant on pages 3-4, line 24; lines 1-2, argues that there is no suggestion or motivation either

in Margulis and/or Patrick references. Examiner's reply: suggestion or motivation: By

integrating the Margulis system controller into Patrick system, that supports a memory

architecture which combines internal and external memory in which common memory can be

used for display memory and main memory, without having inadequate bandwidth access to the

common memory to impair performance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-7, 9-11, 13-17, 19-21, and 22-25 rejected under 35 U.S.C. 103(a) as being

unpatentable over Patrick et al., and further in view of Margulis.

1.   Claim 1,

Patrick et al., hereinafter Patrick, shows a method comprising "writing pixel data to a first

memory location", see disclosure in (Col. 6, lines 15-35) the following example that provides,

what is involved in the block transfer of bytes from a source to a destination in memory. Patrick

also shows "performing a first pixel transformation at said first memory location in a virtual

memory space"; see Fig. 3 is a diagram showing an 8(1, 16, 32) bit per pixel bitmap at a source

(a "source bitmap or first memory location") for transfer to an 8 bpp bitmap at a destination (a

"destination bitmap or second memory location"). Patrick shows a complete illustration of

"generating a memory address for a second memory location", see Fig. 3, that the source bitmap 60 is located at memory addresses 0-499 (decimal) and the destination bitmap 62 is located at memory addresses 900-1399. A data block 61 for transfer is contained within a rectangle 60a in source bitmap 60 and consists of 15 bytes on each of 5 consecutive scan lines at the memory addresses given in the figure. Patrick demonstrates the transformation of data from first location to second location "using a one-way re-mapping to write said transformed pixel data from said first memory location to said second memory location; and transferring said pixel data to a memory controller using a memory controller client in a forward, write-through direction." see Figs. 4-5, data block 61 is to be transferred to a similarly sized rectangle 62a in destination bitmap 62 at the memory addresses given in the figure. Each byte in data block 61 must be fetched (i.e., read) from a source address and written to a destination address. For example, the first byte of the data block has a source address of 19. This byte is to be transferred to a destination address of 905. The next byte for transfer has a source address of 20 and a destination address of 906, and so forth. But Patrick does not explicitly specify mapping, how ever, Margulis teaches in paragraph (0061) from the set and fully associative mapping schemes where a row buffer replacement algorithm must be implemented. Since more than one row buffer can contain the data for a given row access, an algorithm is needed to choose which row buffer to replace for the new access.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Margulis into Patrick et al. in order to improved performance for computationally complex algorithms performed across multiple compute engines. Examiner's suggestion: By integrating the Margulis system controller into Patrick system, that supports a

memory architecture which combines internal and external memory in which common memory

can be used for display memory and main memory, without having inadequate bandwidth access

to the common memory to impair performance.

2.   Claim 11,

Patrick discloses "write pixel data to a first memory location" in (Col. 6, lines 15-35) the

following example that provides, what is involved in the block transfer of bytes from a source to

a destination in memory. Patrick discloses "perform a first pixel transformation at said first

memory location in a virtual memory space" in Fig. 3 is a diagram showing an 8(1, 16, 32) bit

per pixel bitmap at a source (a "source bitmap or first memory location") for transfer to an 8 bpp

bitmap at a destination (a "destination bitmap or second memory location"). The source bitmap

60 is located at memory addresses 0-499 (decimal) and the destination bitmap 62 is located at

memory addresses 900-1399. Patrick discloses "generate a memory address for a second

memory location; use a one-way re-mapping to write said transformed pixel data from said first

memory location to said second memory location; and transferring said pixel data to a memory

controller using a memory controller client in a forward write-through direction." A data block

61 for transfer is contained within a rectangle 60a in source bitmap 60 and consists of 15 bytes

on each of 5 consecutive scan lines at the memory addresses given in the figure. Data block 61

is to be transferred to a similarly sized rectangle 62a in destination bitmap 62 at the memory

addresses given in the figure. Each byte in data block 61 must be fetched (i.e., read) from a

source address and written to a destination address. For example, the first byte of the data block

has a source address of 19. This byte is to be transferred to a destination address of 905. The

next byte for transfer has a source address of 20 and a destination address of 906, and so forth.

But Patrick does not explicitly specify mapping, how ever, Margulis teaches in paragraph (0061)

from the set and fully associative mapping schemes where a row buffer replacement algorithm

must be implemented. Since more than one row buffer can contain the data for a given row

access, an algorithm is needed to choose which row buffer to replace for the new access. Thus, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to

incorporate the teaching of Margulis into Patrick et al. in order to improved performance for

computationally complex algorithms performed across multiple compute engines.

3.   Claim 21,

Patrick demonstrated "A system comprising: a memory controller that receives pixel data and

addresses; a first memory controller client that forwards pixel data and addresses to a first

transfer function; and a second memory controller client that receives data from said first transfer

function together with new addresses." in (Col. 6, lines 15-35) the following example that

provides, what is involved in the block transfer of bytes from a source to a destination in

memory. Fig. 3 is a diagram showing an 8(1, 16, 32) bit per pixel bitmap at a source (a "source

bitmap or first memory location") for transfer to an 8 bpp bitmap at a destination (a "destination

bitmap or second memory location"). The source bitmap 60 is located at memory addresses 0-

499 (decimal) and the destination bitmap 62 is located at memory addresses 900-1399. A data

block 61 for transfer is contained within a rectangle 60a in source bitmap 60 and consists of 15

bytes on each of 5 consecutive scan lines at the memory addresses given in the figure. Data

block 61 is to be transferred to a similarly sized rectangle 62a in destination bitmap 62 at the

memory addresses given in the figure. Each byte in data block 61 must be fetched (i.e., read)

from a source address and written to a destination address. For example, the first byte of the data

block has a source address of 19. This byte is to be transferred to a destination address of 905.

The next byte for transfer has a source address of 20 and a destination address of 906, and so

forth. But Patrick does not explicitly specify mapping, how ever, Margulis teaches in paragraph

(0061) from the set and fully associative mapping schemes where a row buffer replacement

algorithm must be implemented. Since more than one row buffer can contain the data for a given

row access, an algorithm is needed to choose which row buffer to replace for the new access.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to incorporate the teaching of Margulis into Patrick et al. in order to improved performance

for computationally complex algorithms performed across multiple compute engines.

4.   Claim 3,

Patrick illustrated, "The method of claim 1 further including writing pixel data to a

virtual memory location associated with a memory controller client that receives pixel data

written to certain virtual addresses." in Fig. 1, number 40, which is secondary storage area that

can be apply as a virtual memory. (Virtual memory is: extension of the computer's internal

memory, it considers locally or remotely).

5.   Claim 4,

Patrick demonstrated "causing an operating system to set aside virtual addresses for said memory

controller client." And the step is obvious, because the operating system provides this options to

the users to have more memory location as needed it, and these extended memory can be called

virtual memory.

6.   Claim 5,

Patrick demonstrated "generating said memory address for said second memory location

includes transforming the addresses of said pixel data at said first memory location to addresses

at said second memory location." And the step is obvious, because there must be an address to be

able to locate pixel or any other data when transferring pixel data to second memory location.

7.   Claim 6,

Patrick demonstrated "determining the offset to each pixel data by subtracting a base address at

said first memory location from the address of each pixel data." And the step is obvious, because

each memory location has an address tagged to the pixel data, therefore, the pixel data can be

referred to previous location as if the application (recording, viewing, storing) requires. The

memory location will have more space by subtracting a base address from pixel data, but the

pixel data can be viewed once and it depends on the application (player, display once)

requirements.

8.   Claim 7,

Patrick demonstrated "adding said offset to a base address of said second memory location." And

the step is obvious, because the second memory location must have the base address of current

location and plus previous parameters from first memory location (here is offset).

9.   Claim 9,

Patrick demonstrated "writing said transformed pixel data from said first memory location to

said second memory location includes writing said pixel data from said first memory location

associated with a first transfer function to said second memory location associated with a second

transfer function." And the step is obvious, because, Patrick shows in Figs. 5 and 7 that flow

charts of a method for compiling run-time code for a data block transfer.

10.   Claim 10,

Patrick demonstrated "The method of claim 9 including transforming the addresses of said pixel

data from addresses in a first virtual memory range associated with said first transfer function to

memory addresses in a second virtual memory range associated with said second transfer

function." And the step is obvious, because, Patrick shows in Figs. 5 and 7 that flow charts of a

method for compiling run-time code for a data block transfer.

11.   Claim 13,

Patrick illustrated "storing instructions that enable the processor-based system to write pixel data

to a virtual memory location associated with a memory controller client that receives pixel data

written to certain virtual addresses." in Fig. 1, number 40, which is secondary storage area that

can be apply as a virtual memory. (Virtual memory is: extension of the computer's internal

memory, it considers locally or remotely).

12.   Claim 14,

Patrick demonstrated "storing instructions that enable the processor-based system to cause an

operating system to set aside virtual addresses 4 for said memory controller client." And the step

is obvious, because the operating system provides this options to the users to have more memory

location as needed it, and these extended memory can be called virtual memory.

13.   Claim 15,

Patrick demonstrated "storing instructions that enable the processor-based system to transform

the addresses of pixel data at said first memory location to addresses at said second memory

location." And the step is obvious, because there must be an address to be able to locate pixel or

any other data when transferring pixel data to second memory location.

14.   Claim 16,

Patrick demonstrated "storing instructions that enable the processor-based system to determine

the offset to each pixel data by subtracting a base address at said first memory location from the

address of each pixel data." And the step is obvious, because each memory location has an

address tagged to the pixel data, therefore, the pixel data can be referred to previous location as if

the application (recording, viewing, storing) requires. The memory location will have more space

by subtracting a base address from pixel data, but the pixel data can be viewed once and it

depends on the application (player, display once) requirements.

15.   Claim 17,

Patrick demonstrated "storing instructions that enable the processor-based system to add said

offset to a base address of said second memory location." And the step is obvious, because the

second memory location must have the base address of current location and plus previous

parameters from first memory location (here is offset).

16.   Claim 19,

Patrick demonstrated "storing instructions that enable the processor-based system to write said

pixel data from said first memory location associated with a first transfer function to said second

memory location associated with a second transfer function." And the step is obvious, because,

Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code for a

data block transfer.

17.   Claim 20,

Patrick demonstrated "storing instructions that enable the processor-based system to transform

the addresses of said pixel data from addresses in a first virtual memory range associated with

said first transfer function to memory addresses in a second virtual memory range associated

with said second transfer function." And the step is obvious, because, Patrick shows in Figs. 5

and 7 that flow charts of a method for compiling run-time code for a data block transfer.

18.   Claim 22,

Patrick demonstrated "first memory controller client selectively forwards pixel data and

addresses to one of a plurality of transfer functions and said second controller client receives

pixel data with new addresses from said plurality of transfer functions." And the step is obvious,

because, Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code

for a data block transfer.

19.   Claim 23,

Patrick demonstrated "memory controller client writes the pixel data back to said memory

controller." And the step is obvious, because this is the function of memory controller.

20.   Claim 24,

Patrick demonstrated "a plurality of transfer functions, one of said transfer functions arranged to

write output data to an address range of another transfer function." And the step is obvious,

because, Patrick shows in Figs. 5 and 7 that flow charts of a method for compiling run-time code

for a data block transfer.

21.   Claim 25,

Patrick demonstrated "transfer functions are associated with virtual memory address ranges."

And the step is obvious, because the range of memory address must be known in order to be able

to run the transfer function for any type of memory locations.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Javid A Amini whose telephone number is 703-605-4248. The

examiner can normally be reached on 8-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the

organization where this application or proceeding is assigned is 703-746-8705.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is 703-306-0377.

Javid A Amini
Examiner
Art Unit 2672

Javid Amini

JEFFERY BRIER
PRIMARY EXAMINER